

REMARKS

Claims 1-18 were pending and claims 19-37 were withdrawn following Applicants' Election filed October 20, 2005. Claims 19-37 have been cancelled herein as being directed to a non-elected invention. Claims 1, 7, 8, 10, 11, 13, 14 and 17 have been amended and claims 9, 15 and 18 have been cancelled herein. Claims 38 and 39 have been added. Claims 1-8, 10-14, 16-17 and 38-39 are now pending in the present application.

Figure 1 has been objected to for failing to indicate the same as Prior Art. Submitted herewith is a replacement sheet including Figure 1, labeling Figure 1 as Prior Art.

Claims 14 and 17 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Applicants respectfully traverse this rejection.

Claim 14 recites “the first thickness is less than about 400 angstroms, and the second thickness is greater than about 100 angstroms.” The first thickness and the second thickness are specified as ranges. In these ranges, the first thickness and the second thickness can still satisfy the limitation “the second thickness being larger than the first thickness,” as specified in claim 13. Therefore, claim 14 is definite.

For similar reasons, in claim 17, the first thickness and the second thickness are specified as ranges, which do not conflict with the limitation “the second thickness being larger than the first thickness.” As such, claim 17 is definite.

In light of the above discussions, Applicants respectfully submit that claims 14 and 17 are definite, and respectfully request the withdrawal of the rejection to claims 14 and 17.

Claims 1-3, 6-11 and 13 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,911,383 to Doris, et al. (“Doris”).

Claim 1 has been amended herein. It now recites a feature that the multi-gate transistor comprises “a vertical semiconductor fin formed from the second portion of the semiconductor layer; a gate dielectric having vertical portions on opposite sidewalls of a channel portion of the semiconductor fin and a horizontal portion on a top surface of the channel portion of the semiconductor fin; a gate electrode overlying the gate dielectric, wherein the gate electrode has vertical portions on the vertical portions of the gate dielectric and a horizontal portion on the horizontal portion of the gate dielectric.” In Doris, the multiple-gate transistor 32 is a double-gate device comprising two gates on sidewalls of the semiconductor layer 16, and no gate at the top of the semiconductor layer 16. Therefore, Doris lacks the limitation recited in amended claim 1. Claim 1 is thus allowable.

Claims 2-8 and 10-11 are allowable by virtue of their dependence from claim 1, as well as their further defining recitations. Claim 9 has been cancelled herein.

Claim 13 has been amended herein. It now recites “the second transistor is a tri-gate transistor comprising a horizontal gate formed at a top surface of the second portion of the semiconductor layer, and two vertical gates formed at sidewalls of the second portion of the semiconductor layer.” In Doris, the multiple-gate transistor 32 is a double-

gate device having no gate at the top of the semiconductor layer 16. Doris thus lacks the limitation recited in amended claim 13. Claim 13 is thus allowable.

Claims 4-5, 14-15 and 17-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Doris.

Claims 4-5 depend from claim 1, and claim 14 depends from claim 13. Claims 1 and 13 have been amended herein. Since Doris does not teach or suggest the limitation that the multiple-gate transistor is a tri-gate transistor having a gate on a top surface of the semiconductor 32, Doris does not disclose the semiconductor device of amended claims 1 and 13. Accordingly, Applicants respectfully submit that claims 4-5 and 14 are patentable over Doris by virtue of their dependence on claims 1 and 13, respectively, as well as their further defining recitations.

Claim 15 has been cancelled herein.

Claim 17 has been amended and now recites a feature that the second transistor is a multi-gate transistor comprising “a vertical semiconductor fin formed from the second portion of the semiconductor layer; a gate dielectric having at least vertical portions on opposite sidewalls of the semiconductor fin and a horizontal portion on a top surface of the semiconductor fin; a gate electrode overlying the gate dielectric, wherein the gate electrode has vertical portions on the vertical portions of the gate dielectric and a horizontal portion on the horizontal portion of the gate dielectric.” In Doris, the multiple-gate transistor 32 is a double gate device comprising two gates on sidewalls of the semiconductor layer 16, but no gate at the top of the semiconductor layer 16, thus, this

limitation is neither taught nor implied by Doris. Therefore, claim 17 is patentable over Doris.

Claim 18 has been cancelled herein.

Claims 12 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Doris in view of U.S. Publication No. 2002/0011612 to Hieda (“Hieda”).

Claims 12 and 16 depend from claims 1 and 13, respectively. As discussed in preceding paragraphs, Doris lacks the feature that the multi-gate transistor comprises “a vertical semiconductor fin formed from the second portion of the semiconductor layer; a gate dielectric having vertical portions on opposite sidewalls of a channel portion of the semiconductor fin and a horizontal portion on a top surface of the channel portion of the semiconductor fin; a gate electrode overlying the gate dielectric, wherein the gate electrode has vertical portions on the vertical portions of the gate dielectric and a horizontal portion on the horizontal portion of the gate dielectric,” which is recited in amended claim 1. Nowhere does Heida teach or suggest this feature either. Therefore, claim 1, as amended, is patentable over Doris in view of Heida.

Similarly, Doris lacks the limitation “the second transistor is a tri-gate transistor comprising a horizontal gate formed at a top surface of the second portion of the semiconductor layer, and two vertical gates formed at sidewalls of the second portion of the semiconductor layer,” which is recited in claim 13. Nowhere does Heida teach or suggest this limitation either. Therefore, claim 13, as amended, is patentable over Doris in view of Heida.

Accordingly, claims 12 and 16 are allowable over Doris in view of Heida by

virtue of their dependence on respective claims 1 and 13 as well as for their respective further defining recitations.

Claims 7, 8, 10, 11, have been amended due to the amendment to their respective base claims. Claim 14 has been amended to correct an informality.

Claims 38 and 39 have been added to recite that the planar transistor also includes gate portions on sidewalls of the semiconductor layer. Claims 38 and 39 are supported by the specification, for example, Figure 10 of the drawings. No new matter has been added.

In view of the above, Applicants respectfully submit that the application is in condition for allowance and request that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicants request that the Examiner contact Applicants' attorney at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge the appropriate fees to Deposit Account No. 50-1065.

Respectfully submitted,



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